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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,934	03/31/2004	Katsuhisa Matsuda	H-1137	4909

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Mattingly, Stanger & Malur, P.C.
Suite 370
1800 Diagonal Road
Alexandria, VA 22314

EXAMINER	
SITTA, GRANT	
ART UNIT	**PAPER NUMBER**
2629	
MAIL DATE	**DELIVERY MODE**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/812,934	MATSUDA ET AL.	
	Examiner	Art Unit	
	Grant D. Sitta	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/31/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 1 recites the limitation "said first data" and "said second data" in claim 1, lines 3-4 from the bottom. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 2 recites the limitation "the driving pulse" in claim 2, line 3 from the bottom. There is insufficient antecedent basis for this limitation in the claim. It is unclear which driving pulse Applicant is refereeing to, "a driving pulse" from the latch signal in claim 2, line 2 or "a driving pulse" from claim 1, line 9.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-2 and 4-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Koyama et al (US 2002/0024489) hereinafter, Koyama.

7. In regards to claim 1, Koyama teaches an output part (Fig. 1 frame Memory and Data comparison circuit, refresh generating circuit, and clock generation) for outputting an electrode driving pulse (Fig. 4) for driving said address electrode of said display device [para 0001] according to a first change-over signal ([0009]-[0011] first signal sent into the data comparison circuit), a second change-over signal ([0009]-[0011]], second signal sent to the data comparison circuit), and a driving pulse ([0009]-[0011] signal from source driver) and an output driving part (Fig. 1 source driver and gate driver) for driving said output part according to said display data (Fig. 1 "video signal"),

wherein said output driving part (Fig. 1 source driver and gate driver) outputs the driving pulse (fig.1 signal from drivers); for driving said output part (Fig. 1 frame Memory and Data comparison circuit, refresh generating circuit, source driver, gate driver and clock generation) when said first data inputted (Fig. 1 signal from S1 to memory 1) first

and said second data inputted (Fig. 1 signal from S1 to memory 2) after the input of said first data come to change both of said first and second data being included in said display data [0009]-[0011].

8. In regards to claim 2, Koyama teaches a driving pulse generation (Fig. 1 "clock generation") part for generating a driving pulse (fig. 1 clock pulse) from a latch signal (fig. 2 signal to latch); a shift register (Fig. 2, "Shift register 1") for shifting inputted display data according to a shift pulse (Fig. 2 "clock data"), then outputting said shifted display data; a first latch for latching display data (Fig. 2, "Latch 1") output from said shift register (Fig. 2, "Shift register 1") according to the latch signal (fig. 2 signal to latch); a second latch (Fig. 2, "Latch 2") for latching display data output from said first latch (Fig. 1, "Latch 1") according to the driving pulse (Fig. 1 clock pulse); and a driving pulse output part for comparing (Fig. 2 "EXOR" and "OR" gates) said first data output from said first latch (Fig. 1, "Latch 1") with said second data output from said second latch (Fig. 2, "Latch 2"), then outputs the driving pulse (fig.1 refresh pulse) to said output part when said first data does not match with said second data ([0058]).

9. In regards to claim 4, Koyama teaches a semiconductor integrated circuit device for driving an address electrode of a display device according to display data, wherein said semiconductor integrated circuit device includes a driving control part (Fig. 1 frame Memory and Data comparison circuit, refresh generating circuit, clock generation and memory controller) that includes an output part (Fig. 1 source driver and gate driver) for

outputting an electrode driving pulse (Fig. 1 signal from source driver and gate driver) for driving said address electrode (Fig. 1 (1,2.....M)) of said display device and an output driving part (Fig. 1 source driver and gate driver) for driving said output part ((Fig. 1 frame Memory and Data comparison circuit, refresh generating circuit, clock generation and memory controller)according to said display data, and

wherein said output driving part (Fig. 1 source driver and gate driver) converts the output of said output part (Fig. 1 frame Memory and Data comparison circuit, refresh generating circuit, source driver, clock generation and memory controller) into a high impedance state (inherent when driving high impedance displays [0096]) according to a high impedance control signal (clock) when an output state of said output part is changed over [0009]-[0011].

10. In regards to claim 5, Koyama teaches wherein said output driving part includes: a shift register (inherent in source and gate driver) for shifting inputted display data according to a shift pulse (inherent from shift registers inside source and gate drivers), then outputting the shifted display data [0063];

and a first latch (inherent in source and gate drivers) for latching display data output from said shift register according to a latch signal (fig. 2 signal to latch); and

wherein said driving control part includes: a signal generation part (fig. 2) for generating first (fig. 2 signals from shift register 1) and second delay signals (fig. 2

signal from shift register 2) of which timings are different from each other [0058] according to latch signals (fig. 2 signal to latch);

a first driving pulse generation part (fig. 2 shift register 1) for generating a first driving pulse according to the first delay signal output from said signal generation part [0057];

a second driving pulse generation part (fig. 2 shift register 2) for generating a second driving pulse according to the second delay signal output from said signal generation part (frame memory) [0057];

a first selector (fig. 2, "EXOR" (1)) for selecting either said first delay signal (fig. 2 signal from latch 1) or second delay signal (fig. 2 signal from latch 2) output from said signal generation part (frame memory) according to an output signal output from said first latch (latch 1) and the first selector (fig. 2, "EXOR") for outputting the selected delay signal as a first or second change-over signal; and

a second selector (fig. 2, "OR" circuit) for selecting one of said first (fig. 2 shift register 1) and second (fig. 2 shift register 2) driving pulses output from said first and second driving pulse generation parts (fig. 2 shift register 1 and 2) according to an output signal output from said first latch (latch 1) and the second selector (fig. 2, "OR" circuit) for outputting the selected driving pulse as a driving pulse [0058].

11. In regards to claim 6, Koyama teaches where the output driving part ((Fig. 1 frame Memory and Data comparison circuit, refresh generating circuit, clock generation and memory controller) outputs the driving pulse for driving said output part (Fig. 1 source driver and gate driver) when first data (Fig. 1 signal from S1 to memory 1) inputted first and second data inputted (Fig. 1 signal from S1 to memory 2) after the input of said first data come to change both of said first and second data being included in said display data [0009]-[0011].

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koyama in view of Shino et al (US 6,118,220), hereinafter, Shino.

15. In regards to claim 3 and 7, Koyama discloses the limitations of claim 1

Koyama differs from the claimed invention in that Koyama does not explicitly disclose a conventional scanning electrode driving circuit.

However, Shino shows a conventional scanning electrode driving circuit including a push-pull circuit (fig. 6 (13) and (14)) in which first (13) and second transistors (14) are coupled serially between a first supply voltage (ground) and a reference potential (-200v); a level shift circuit (15) including a differential amplification circuit (inherent with a level shift circuit) driven by said first supply voltage (ground) and the level shift circuit (15) driving said first transistor (13) that is a pull-up element of said output circuit (fig. 6) according to said first change-over signal ([0009]-[0011] first signal sent into the data comparison circuit, Koyama), and said driving pulse (fig.1 signal from source driver and gate driver); and a driving part driven by a second supply voltage (inherent with a level shift circuit) having a voltage value lower than that of said first supply voltage and the driving part driving said second transistor that is a pull-down ((14), Shino) element of said output circuit (Fig. 6, Shino) according to said second change-over signal ([0009]-[0011]], second signal sent to the data comparison circuit, Koyama) and (col. 5, lines 25-50 of Shino).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Koyama to include the use of a conventional scanning electrode

driving circuit as shown by Shino in order to drive a display as stated in (col. 6, lines 25-50 of Shino).

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The US 2002/0015032 is cited to teach a holding of a digital image signal where a sampling pulse is wider than a pulse width input from the outside and both signals are included in the output of the sampling pulse. The US 6,414,670 is cited to teach a LCD driving method, which can minimize power consumption by avoiding unnecessary driving of gate line drivers. The US 5,003,228 is cited to teach a method to drive a plasma display that can reduce power consumption that utilizes shift registers, latch, and a push-pull circuit.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Grant D. Sitta whose telephone number is 571-270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-270-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Grant D. Sitta

June 4, 2007

XIAO WU
SUPERVISORY PATENT EXAMINER